IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of	:	**Mail Stop Amendment**
Gyung-su Byon	:	Group Art Unit: 2827
Application No. 10/758,539	:	Examiner: Le, Thong Quoc
Filed January 16, 2004	:	

Title: SEMICONDUCTOR DEVICE INCLUDING DUTY CYCLE CORRECTION CIRCUIT

REQUEST FOR RECONSIDERATION

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria VA 22314

Sir:

This is in response to the Office Action dated January 18, 2006.

Claims 1-13 remain pending in the application.

Allowable Claims

Applicants acknowledge with thanks the indicated allowability of the subject matter of claims 2-5 and 8-13.

35 U.S.C. ¶102

Claims 1 and 6-7 were rejected under 35 U.S.C. ¶102 as being anticipated by Donnelly et al. (US 5945862) for the reasons stated at pages 2-3 of the Office Action. Since Donnelly et al. does not teach or suggest at least the claimed control circuit that controls the respective slew rates of the first and second clock signals "by adjusting capacitance values of first and second input

terminals receiving the first and second clock signals", Applicants respectfully traverse this rejection.

In the Office Action the Examiner states:

> *"Regarding claim 1, Donnelly et al. disclosed a semiconductor device (Figure 13), comprising: a duty cycle correction (DCC) circuit (Figure 17) that receives first and second clock signals (Figure 17, 2305, 2310) and outputs a duty cycle adjusted clock signal (Figure 17, DCC); ... ."*

It appears that the Examiner has equated the clock signals CLOCK and CLOCK_B of the circuit illustrated in FIG. 17 of Donnelly et al. to the first and second clock signals of claim 1 of the present application. It is noted, however, that FIG. 17 of Donnelly et al. does not illustrate the duty cycle correction (DCC) circuit as apparently suggested by the Examiner. Rather, FIG. 17 illustrates an embodiment of the duty cycle error detector 1625 shown in FIG. 13. Please see col. 9, line 55, of Donnelly et al. As discussed below, the error detector 1625 produces differential error voltages DCC and DCCB, and does not output a duty cycle adjusted clock signal as stated by the Examiner.

In the Office Action, the Examiner further states:

> *"wherein the control circuit [of Donnelly et al.] controls the respective slew rates of the first and second clock signals (Column 8, lines 44-62) by adjusted capacitance values (Figure 17, 2370, 2375) of first and second input terminals receiving the first and second clock signals respectively (Figure 17)."*

The Examiner appears to have misinterpreted the teachings of Donnelly et al. Attention is respectfully directed to the following passage appearing at column 6, lines 44-53, of Donnelly et al.:

> *"Duty cycle error detector 1625 produces a pair of differential error voltages DCC 1650 and DCCB 1645 which are received by duty cycle control converter 1615 which in turn produces pull up bias voltage Vcp 1660 and pull down bias voltage Vcn 1655. Multiplexor 1610 receives the pull up and pull down bias voltages and corrects the duty cycle out the output signal 1630 producing a corrected clock on line 1630. In operation, assuming that the output clock has a high time that is greater than 50%, the duty cycle error detector 1625 determines that the high time of the clock is too large and indicates this condition by setting the DCC signal 1650 to be larger than DCCB signal 1645."*

As is apparent from the above, the duty cycle correction is executed by the multiplexor 1610 illustrated in FIG. 13 of Donnelly et al. The duty cycle error detector 1625 simply produces differential error voltages DCC and DCCB depending upon whether the output clock duty cycle is less than or greater than 50%.

The duty cycle correction functionality (i.e., slew rate adjustment) of the multiplexor 1610 is achieved by the circuit block 2160 illustrated in FIG. 15 of Donnelly et al. As shown, transistors P1 and N1 are responsive to the pull-up and pull-down bias voltages Vcp and Vcn to adjust the fall time of the signal output from the multiplexor elements 2100. The "slew-rate altered signal" is then applied to the buffer 2140 of FIG. 15. Please see col. 9, lines 33-44, of Donnelly et al.

Donnelly et al. therefore does not teach or suggest the claimed control circuit that controls the respective slew rates of the first and second clock

signals "by adjusting capacitance values of first and second input terminals receiving the first and second clock signals" as recited in claim 1.

The Examiner has made reference to the capacitors 2370 and 2375 of the detector circuit of FIG. 17. However, these capacitors are not adjustable, nor are they connected to the input terminals of the clock signals CLOCK and CLOCK_B. Further, as discussed above, the detector circuit of FIG. 17 does not function to control slew rates of the clock signals CLOCK and CLOCK_B.

For at least the reasons stated above, Applicants respectfully contend that claims 1 and 6-8 define over the teachings of Donnelly et al.

Conclusion

No other issues remaining, reconsideration and favorable action upon the claims 1-13 now pending in the application are requested.

Respectfully submitted,

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